REMARKS:

In the Office Action mailed December 2, 2003 the Examiner noted that claims 11-26 are pending, and that claims 11-26 have been rejected. Claims 11, 15, 17, 19, 20, 22 and 23 have been amended, and new claims 27-29 have been added.

Per our November 20, 2003 interview with the Examiner, the dependency of claims 17, 20, and 22 has been amended to depend from claims 15 and 19. Specifically, claim 17 depends from claim 15, and both claims 20 and 22 depend from claim 19. No new matter has been added. The Examiner's rejections are traversed below.

REJECTION UNDER 35 U.S.C. §102(e):

In the outstanding Office Action, claims 11,12,14-16,18-20,22-24, and 26 were rejected under 35 U.S.C. § 102(e) as being taught by U.S. Patent No. 5,930,492 ('492). The rejection is traversed and reconsideration is respectfully requested.

'492 discusses a method and apparatus for performing control within pipeline stages and routing between the pipeline stages using a control and a steering word. Accordingly, pipeline modifications are made by modifying the corresponding control and steering word of the pipeline stages.

The present application is directed to a processor execution pipeline particularly to the execution stage of numerous stages that exist in a processor to reduce the amount of hardware required and the amount of power consumed while achieving high-speed processing.

The Examiner compares the control and steering word of '492 used to specify control signals for instructions at each pipeline stage and route the instructions through the pipeline stages to the instruction decoding unit of the present application. The instruction processing pipeline method of '492 uses the control word to dictate an operation to be performed at each pipeline stage (see, column 3, lines 36-39 of '492) and uses the steering word to dictate which pipeline stage receives the instruction (see, column 3, lines 39-40 of '492). Accordingly, the pipeline stages of '492 are coupled to receive (see, column 3, lines 8-10 of '492) and produce a control word and a steering word (see, column 3, lines 28-32) upon receipt of a control and a steering word from another pipeline stage. As stated in '492, the use of the control and steering word eliminates the need to use decode logic within each pipeline stage (see, column 2, lines 4-18, 41-47 of '492).

In contrast, as recited in amended claims 11, 15, 19, and 23, the first instruction

decoding unit of the present application "decodes a first instruction into a first control signal, and decodes **all other** instructions with the exception of the first instruction into a second control signal when the first instruction is decoded into a first control signal". Similarly, the second instruction decoding unit "decodes a second instruction into a third control signal, and decodes **all other** instructions with the exception of the second instruction into a fourth control signal when the second instruction is decoded into the third control signal" (see, FIG. 2 of the present application). This allows data to be passed through the respective processing units at the time the corresponding instruction is decoded to the processing unit, thereby allowing latching units to be shared by the execution stages to reduce the amount of hardware required and power consumed during the high-speed processing. And unlike the apparatus of '492 that couples an input operand to the steering and control word, the present application translates and "decodes" one kind of instruction into a control signal and translates "all other instructions" into another control signal to control a processor execution pipeline (see, claims 11, 15, 19, and 23 of the present application). Thus, the instruction decoding units of the present application that translate the instructions are not comparable to the control and steering word of '492 that are merely added to an input operand.

Further, the present application comprises "a multiplexer that selects an output of the second processing unit or the second data" (see, claims 12,15,16,18, 20, 23, 24, and 26 of the present application). The multiplexer allows the selection of output processed via the second processing unit or the first processing unit based on the control signal received. This is unlike the method of '492 that selects from inputs of the pipeline stages based on the selection control asserted (see, column 20, line 66 – column 21, line 14 of '492). Thus, according to '492, there are different combinations of stages that the control words may pass through as the control words can enter instruction pipeline at any one of the stages and can also exit the pipeline at any stage (see, column 20, 19-28 of '492). However, according to an aspect of the present application, the processor execution pipeline relates to the execution stage of a process.

Thus, the processor execution method of the present application is not anticipated by the pipeline control using control and steering word method of '492.

REJECTION UNDER 35 U.S.C. § 103(a):

In the outstanding Office Action, claims 13, 17, 21, and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over '492 in view of InstantWeb's Free Online Computing Dictionary. The rejection is traversed and reconsideration is respectfully requested.

The Examiner acknowledges that '492 does not teach a latching unit that holds the output of the first processing unit where the second data is data held by the latching unit. However, the Examiner relies on an Internet definition of "latch" and the dataflow elements of '492 to reject claims 13, 17, 21, and 25. The dataflow elements of '492 perform an operation upon an input operand to produce a result operand to be conveyed to the next pipeline stage (see, column 22, lines 61-65 of '492). The control signals used by each dataflow element are provided from the control word received by the first pipeline stage (see, column 22, lines 57-60 of '492). The pipeline control method of '492 does not discuss "a latching unit that holds the output of the first processing unit [the multiplexer] where the second data is data held by the latching unit" (see, claims 13, 17, 21, and 25 of the present application), the output being outputted when the decoded second control signal is received from the first instruction decoding unit that decodes all other instructions with the exception of the first instruction into a second control signal (see, independent claims 11, 15, 19, and 23 from which claims 13, 17, 21, and 25 depend).

The burden of establishing a prima facie case of obviousness based upon the prior art lies with the Examiner. In re Fritch, 23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992). According to In re Fritch, the Examiner "... can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." Since '492 does not mention holding or storing an output of a processing unit when a certain condition is met, there is no motivation to combine the dataflow elements '492 method to a latch unit as defined in the InstantWeb's Free Online Computing Dictionary. As emphasized by the amended claims, the different aspects of the present application are mainly directed to the execution stage in a processor and not other preceding and subsequent stages in the process.

Accordingly, withdrawal of the rejection is requested.

NEW CLAIMS:

New claims 27 and 29 has been added to clarify that the present application is mainly directed to the execution stage of the various stages in a processor, which allows stage latch circuits to be shared. As recited in claim 27, "the latching unit holds the output of the first processing unit and the second data is data held by the latching unit allowing the latching unit to be shared by the first and second processing units". Specifically, the latching unit holds both the first data, which is output by the first processing unit, and second data accessible by the second

processing unit, allowing first and second processing units to share the stage latch circuit.

New claim 28 has been added to emphasize a processor execution pipeline method "decoding a first instruction into a first control signal, and decoding all other instructions with the exception of the first instruction into a second control signal" and "decoding a second instruction into a third control signal, and decoding all other instructions with the exception of the second instruction into a fourth control signal" (see also, claim 29). Accordingly, allowing data to be passed through the respective processing units at the time the corresponding instruction is decoded to the processing unit.

CONCLUSION

In accordance with the foregoing amendments and remarks, it is submitted that claims 11-29 patentably distinguish over the references cited by the Examiner. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: 5/3/4

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